8-Channel, 1 MSPS, 8- /10- /12- Bit ADCs with Sequencer in 20-Lead TSSOP

AD7908/AD7918/AD7928

FEATURES

Fast throughput rate: 1 MSPS
Specified for AV_{DD} of 2.7 V to 5.25 V
Low power
6.0 mW max at 1 MSPS with 3 V supply
13.5 mW max at 1 MSPS with 5 V supply
Eight (single-ended) inputs with sequencer
Wide input bandwidth
AD7928, 70 dB min SINAD at 50 kHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface SPI®/QSPI™/
MICROWIRE™/DSP compatible
Shutdown mode: 0.5 µA max
20-lead TSSOP package

GENERAL DESCRIPTION

The AD7908/AD7918/AD7928 are, respectively, 8-bit, 10-bit, and 12-bit, high speed, low power, 8-channel, successive approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1 MSPS. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 8 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7908/AD7918/AD7928 use advanced design techniques to achieve very low power dissipation at maximum throughput rates. At maximum throughput rates, the AD7908/AD7918/AD7928 consume 2 mA maximum with 3 V supplies; with 5 V supplies, the current consumption is 2.7 mA maximum.

Through the configuration of the control register, the analog input range for the part can be selected as 0 V to REF_{IN} or 0 V to 2 × REF_{IN}, with either straight binary or twos complement output coding. The AD7908/AD7918/AD7928 each feature eight single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially.

The conversion time for the AD7908/AD7918/AD7928 is determined by the SCLK frequency, which is also used as the master clock to control the conversion.

FUNCTIONAL BLOCK DIAGRAM

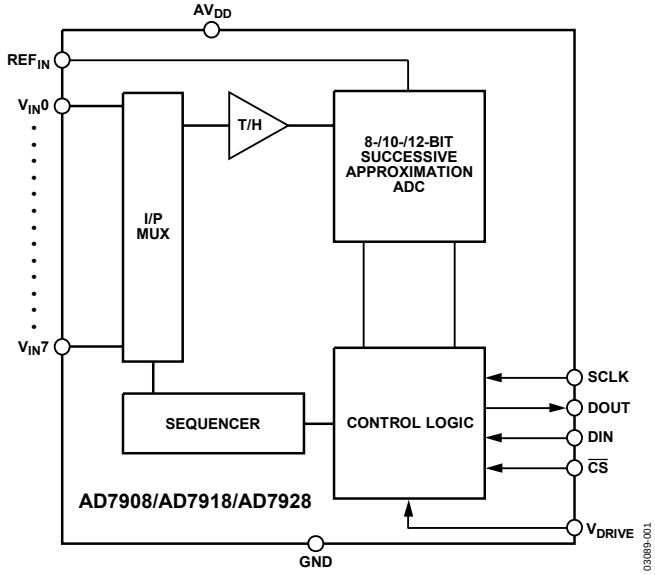

Figure 1.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption. The AD7908/AD7918/AD7928 offer up to 1 MSPS throughput rates. At the maximum throughput rate with 3 V supplies, the AD7908/AD7918/AD7928 dissipate just 6 mW of power maximum.

2. Eight Single-Ended Inputs with a Channel Sequencer. A sequence of channels can be selected, through which the ADC cycles and converts on.

3. Single-Supply Operation with V_{DRIVE} Function. The AD7908/AD7918/AD7928 operate from a single 2.7 V to 5.25 V supply. The V_{DRIVE} function allows the serial interface to connect directly to either 3 V or 5 V processor systems independent of AV_{DD}.

4. Flexible Power/Serial Clock Speed Management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. The parts also feature various shutdown modes to maximize power efficiency at lower throughput rates. Current consumption is 0.5 µA max when in full shutdown.

5. No Pipeline Delay. The parts feature a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

6/06—Rev. A to Rev. B

Updated Format ... Universal
Changes to Reference Section ... 21

9/03—Rev. 0 to Rev. A

Changes to Figure 3 ... 15
Changes to Reference section ... 18

SPECIFICATIONS

AD7908 SPECIFICATIONS

AV_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal-to-(Noise + Distortion) (SINAD)[2]	49	dB min	
Signal-to-Noise Ratio (SNR)[2]	49	dB min	
Total Harmonic Distortion (THD)[2]	−66	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	−64	dB max	
Intermodulation Distortion (IMD)[2]			fa = 40.1 kHz, fb = 41.5 kHz
Second-Order Terms	−90	dB typ	
Third-Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY[2]			
Resolution	8	Bits	
Integral Nonlinearity	±0.2	LSB max	
Differential Nonlinearity	±0.2	LSB max	Guaranteed no missed codes to 8 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error	±0.5	LSB max	
Offset Error Match	±0.05	LSB max	
Gain Error	±0.2	LSB max	
Gain Error Match	±0.05	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error	±0.2	LSB max	
Positive Gain Error Match	±0.05	LSB max	
Zero Code Error	±0.5	LSB max	
Zero Code Error Match	±0.1	LSB max	
Negative Gain Error	±0.2	LSB max	
Negative Gain Error Match	±0.05	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to REF_{IN}	V	RANGE bit set to 1
	0 to 2 × REF_{IN}	V	RANGE bit set to 0, AV_{DD}/V_{DRIVE} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 1 MSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

Parameter	B Version[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (natural) binary		Coding bit set to 1
	Twos complement		Coding bit set to 0
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time	300	ns max	Sine wave input
	300	ns max	Full-scale step input
Throughput Rate	1	MSPS max	See Serial Interface section
POWER REQUIREMENTS			
AV_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}[4]			Digital inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	600	µA typ	AV_{DD} = 2.7 V to 5.25 V, SCLK On or Off
Normal Mode (Operational)	2.7	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Using Auto Shutdown Mode	960	µA typ	f_{SAMPLE} = 250 kSPS
	0.5	µA max	(Static)
Full Shutdown Mode	0.5	µA max	SCLK on or off (20 nA typ)
Power Dissipation[4]			
Normal Mode (Operational)	13.5	mW max	AV_{DD} = 5 V, f_{SCLK} = 20 MHz
	6	mW max	AV_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode (Static)	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V

[1] Temperature ranges as follows: B version: –40°C to +85°C.
[2] See Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] See Power vs. Throughput Rate section.

AD7918 SPECIFICATIONS

AV_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal-to-(Noise + Distortion) (SINAD)[2]	61	dB min	
Signal-to-Noise Ratio (SNR)[2]	61	dB min	
Total Harmonic Distortion (THD)[2]	−72	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	−74	dB max	
Intermodulation Distortion (IMD)[2]			fa = 40.1 kHz, fb = 41.5 kHz
Second-Order Terms	−90	dB typ	
Third-Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY[2]			
Resolution	10	Bits	
Integral Nonlinearity	±0.5	LSB max	
Differential Nonlinearity	±0.5	LSB max	Guaranteed no missed codes to 10 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error	±2	LSB max	
Offset Error Match	±0.2	LSB max	
Gain Error	±0.5	LSB max	
Gain Error Match	±0.2	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error	±0.5	LSB max	
Positive Gain Error Match	±0.2	LSB max	
Zero Code Error	±2	LSB max	
Zero Code Error Match	±0.2	LSB max	
Negative Gain Error	±0.5	LSB max	
Negative Gain Error Match	±0.2	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to REF_{IN}	V	RANGE bit set to 1
	0 to 2 × REF_{IN}	V	RANGE bit set to 0, AV_{DD}/V_{DRIVE} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 1 MSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

Parameter	B Version[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (natural) binary		Coding bit set to 1
	Twos complement		Coding bit set to 0
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time	300	ns max	Sine wave input
	300	ns max	Full-scale step input
Throughput Rate	1	MSPS max	See Serial Interface section
POWER REQUIREMENTS			
AV_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}[4]			Digital inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	600	µA typ	AV_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational)	2.7	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Using Auto Shutdown Mode	960	µA typ	f_{SAMPLE} = 250 kSPS
	0.5	µA max	(Static)
Full Shutdown Mode	0.5	µA max	SCLK on or off (20 nA typ)
Power Dissipation[4]			
Normal Mode (Operational)	13.5	mW max	AV_{DD} = 5 V, f_{SCLK} = 20 MHz
	6	mW max	AV_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode (Static)	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V

[1] Temperature ranges as follows: B version: –40°C to +85°C.
[2] See Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] See Power vs. Throughput Rate section.

AD7928 SPECIFICATIONS

A_{VDD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal-to-(Noise + Distortion) (SINAD)[2]	70	dB min	@ 5 V
	69	dB min	@ 3 V typically 70 dB
Signal-to-Noise Ratio (SNR)[2]	70	dB min	
Total Harmonic Distortion (THD)[2]	−77	dB max	@ 5 V typically −84 dB
	−73	dB max	@ 3 V typically −77 dB
Peak Harmonic or Spurious Noise	−78	dB max	@ 5 V typically −86 dB
(SFDR)[2]	−76	dB max	@ 3 V typically −80 dB
Intermodulation Distortion (IMD)[2]			fa = 40.1 kHz, fb = 41.5 kHz
Second-Order Terms	−90	dB typ	
Third-Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY[2]			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error	±8	LSB max	Typically ±0.5 LSB
Offset Error Match	±0.5	LSB max	
Gain Error	±1.5	LSB max	
Gain Error Match	±0.5	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error	±1.5	LSB max	
Positive Gain Error Match	±0.5	LSB max	
Zero Code Error	±8	LSB max	Typically ±0.8 LSB
Zero Code Error Match	±0.5	LSB max	
Negative Gain Error	±1	LSB max	
Negative Gain Error Match	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to REF_{IN}	V	RANGE bit set to 1
	0 to 2 × REF_{IN}	V	RANGE bit set to 0, AV_{DD}/V_{DRIVE} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 1 MSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

Parameter	B Version[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (natural) binary		Coding bit set to 1
	Twos complement		Coding bit set to 0
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time	300	ns max	Sine wave input
	300	ns max	Full-scale step input
Throughput Rate	1	MSPS max	See Serial Interface section
POWER REQUIREMENTS			
AV_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}[4]			Digital inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	600	µA typ	AV_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational)	2.7	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Using Auto Shutdown Mode	960	µA typ	f_{SAMPLE} = 250 kSPS
	0.5	µA max	(Static)
Full Shutdown Mode	0.5	µA max	SCLK on or off (20 nA typ)
Power Dissipation[4]			
Normal Mode (Operational)	13.5	mW max	AV_{DD} = 5 V, f_{SCLK} = 20 MHz
	6	mW max	AV_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Shutdown Mode (Static)	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V

[1] Temperature ranges as follows: B Version: −40°C to +85°C.
[2] See Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] See Power vs. Throughput Rate section.