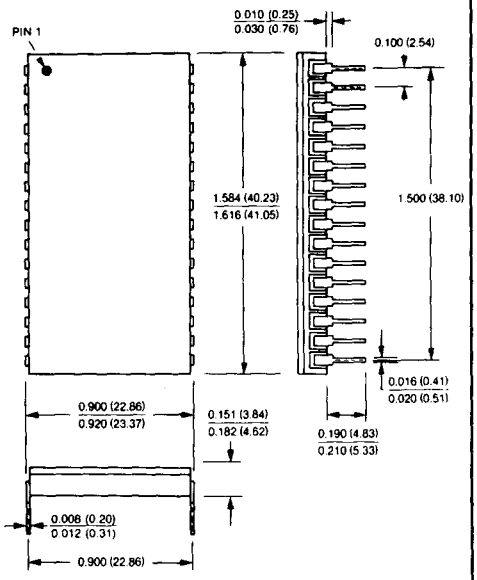
12-bit, 8μsec Military A/D Converter

FEATURES

- Fully Guaranteed −55°C to +125°C Operation
- 8μsec Max Conversion Time
- Complete/Versatile A/D Function:
  - Internal or External Clock
  - Internal Reference
  - User-Optional Input Buffer
  - Serial and Parallel Outputs
  - Short-Cycle Pin
- No Missing Codes Guaranteed Over Temperature
- Low Drift:
  Gain ±20ppm/°C Max
  Offset ±5ppm/°C Max
- Pin-Compatible ADC84/85
- MIL-PRF-38534 Screening Optional.



Dimensions in Inches
(millimeters)

DESCRIPTION

The Micro Networks ADC87 is a high-performance, 12-bit, successive approximation, A/D converter in a hermetically sealed, ceramic, 32-pin dual-in-line package. It is pin-compatible with industry-standard ADC85 type 12-bit A/D converters and is the first device of this type to offer fully guaranteed performance specifications over the full -55°C to +125°C operating temperature range. It also guarantees an 8μsec max conversion time compared to the 10μsec of other devices in its class. ADC87 linearity is guaranteed better than ±½LSB, and no missing codes is guaranteed over temperature. Max gain drift is a low ±20ppm/°C; max offset drift a low ±5ppm of FSR/°C.

ADC87 is extremely versatile. It has its own reference and internal clock; yet it can run from an external clock. There are 5 user-selectable input ranges, serial and parallel outputs, a short-cycle pin, a user-optional high-impedance input buffer and pins for optional offset and gain adjustments.

For military aerospace or harsh-environment commercial/industrial applications, ADC87H/B CH is fully screened to MIL-PRF-38534.

ADC87 is ideally suited for fast data digitizing in military/aerospace applications. Its rugged, hermetically sealed, ceramic package has outstanding thermal characteristics and can withstand the harshest environments.

ADC87 12-Bit 8μsec A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
ADC87	−25°C to +85°C
ADC87H, ADC87H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 28)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 31)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 16)	−0.5 to +7 Volts
Digital Inputs (Pins 14, 21)	−0.5 to +5.5 Volts
Analog Inputs: Direct (Pins 24, 25)	±25 Volts
Buffer (Pin 30)	±15 Volts

ORDERING INFORMATION

PART NUMBER ADC87H/B CH

Standard part is specified for −25°C to +85°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-PRF-38534.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +5, 0 to +10		Volts
Bipolar		±2.5, ±5, ±10		Volts
Direct Input Impedance (Note 1): 0 to +5V, ±2.5V		2.5		kΩ
0 to +10V, ±5V		5		kΩ
±10V		10		kΩ
Buffer Amplifier (Note 2): Gain Accuracy		±0.01		%
Input Impedance (Note 1)	10^{10}	10^{12}		Ω
Input Bias Current (Note 1)		±2	±7	nA
Offset Voltage		±4	±10	mV
Settling Time (20V Step to ±0.01%FSR)		3		μsec
DIGITAL INPUTS (Start Convert, Short Cycle)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+80	μA
Logic "0" (V_{IL} = +0.4V)			−3.2	mA
TRANSFER CHARACTERISTICS (Note 3)				
Linearity Error: Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 4)		±½	±1	LSB
Differential Linearity Error		±½		LSB
Differential Linearity Drift (Notes 1, 4)		±2		ppm of FSR/°C
Guaranteed Temperature Range for No Missing Codes:				
ADC87	−25		+85	°C
ADC87H, ADC87H/B	−55		+125	°C
Unipolar Offset Error (Notes 5, 6): Initial (+25°C)		±0.1	±0.2	%FSR
Drift (Note 4)		±3	±5	ppm of FSR/°C
Bipolar Zero Error (Notes 5, 7): Initial (+25°C)		±0.1	±0.25	%FSR
Drift (Note 4)		±5	±10	ppm of FSR/°C
Gain Error (Notes 5, 8): Initial (+25°C)		±0.1	±0.25	%
Drift (Note 4)		±10	±20	ppm/°C
DIGITAL OUTPUTS (Parallel, Serial, Clock, Status)				
Output Coding (Note 9): Unipolar Ranges		CSB		
Bipolar Ranges		COB, CTC		
Logic Levels: Logic "1" ($I_{SOURCE} \leq 40\mu A$)	+2.4			Volts
Logic "0" ($I_{SINK} \leq 1.6mA$)			+0.4	Volts
REFERENCE OUTPUT				
Internal Reference: Voltage		+6.3		Volts
Accuracy (Note 1)		±5		%
Tempco		±5	±10	ppm/°C
External Current			200	μA

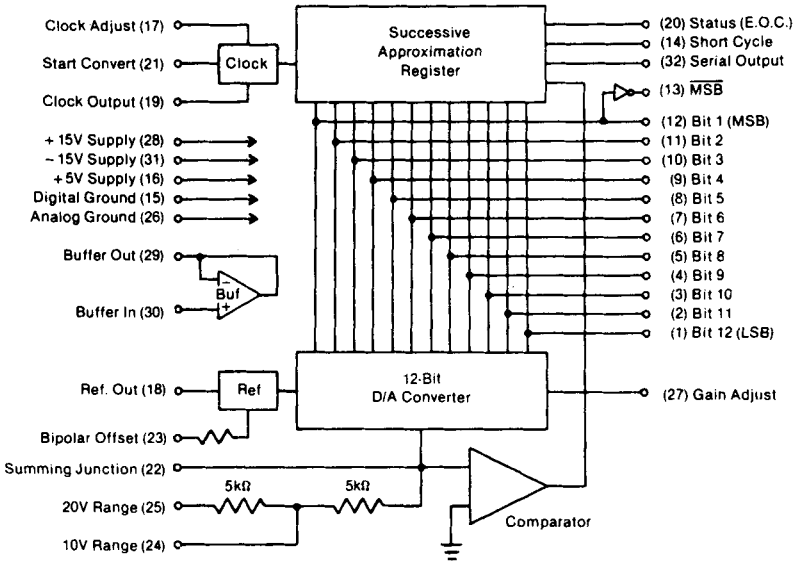
DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (Note 10)		7	8	μsec
Internal Clock Frequency (Note 1)	1.5	1.7		MHz
Start Convert Pulse Width (Note 1)	50			nsec
Delay Falling Edge of Start Convert to Status="1" (Note 1)		50	100	nsec
Delay Falling Edge of Status to LSB Valid (Note 1)		25	120	nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status)		75	140	nsec
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.5	+15	+15.5	Volts
−15V Supply	−14.5	−15	−15.5	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Note 11): +15V Supply		±0.01	±0.02	%FSR/%Supply
−15V Supply		±0.01	±0.02	%FSR/%Supply
+5V Supply		±0.005	±0.01	%FSR/%Supply
Current Drain: +15V Supply		+27	+35	mA
−15V Supply		−27	−35	mA
+5V Supply		+60	+75	mA
Power Consumption		1110	1425	mW

SPECIFICATION NOTES:

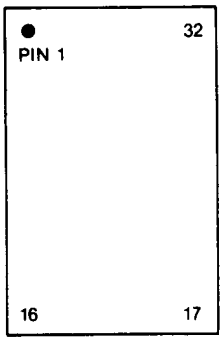
1. These parameters are listed for reference only and are not tested.
2. When using the internal buffer amplifier, buffer settling time must be added to conversion time when calculating system throughput. See section labled Internal Buffer Amplifier.
3. FSR = full scale range. A unit connected for a 0 to +5V or ±2.5V input range has a 5V FSR. A unit connected for a 0 to +10V or ±5V input range has a 10V FSR, etc.. 1 LSB for 12 bits is equivalent to 0.024%FSR.
4. Listed specification applies over the −25°C to +85°C temperature range for ADC87. Listed specification applies over the −55°C to +125°C temperature range for ADC87H and ADC87H/B.
5. Initial error is adjustable to zero.
6. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 when operating the ADC87 on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
7. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the ADC87 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
8. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.
9. CSB = complementary straight binary. COB = complementary offset binary. CTC = complementary two's complement. See table of transition voltages in section labeled Digital Output Coding.
10. Conversion is initiated on the falling edge of the start convert command, and conversion time is defined as the width of status (E.O.C.). Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 2 (Bit 11) to pin 14 (Short Cycle) for 10-bit conversions. See Timing Diagram.
11. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



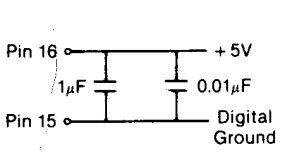
1	Bit 12 (LSB)	32	Serial Output
2	Bit 11	31	−15V Supply (−Vcc)
3	Bit 10	30	Buffer Input
4	Bit 9	29	Buffer Output
5	Bit 8	28	+15V Supply (+Vcc)
6	Bit 7	27	Gain Adjust
7	Bit 6	26	Analog Ground
8	Bit 5	25	20V Range
9	Bit 4	24	10V Range
10	Bit 3	23	Bipolar Offset
11	Bit 2	22	Summing Junction
12	Bit 1 (MSB)	21	Start Convert
13	$\overline{\text{MSB}}$	20	Status (E.O.C.)
14	Short Cycle	19	Clock Output
15	Digital Ground	18	Reference Output (+6.3V)
16	+5V Supply (+Vdd)	17	Clock Adjust

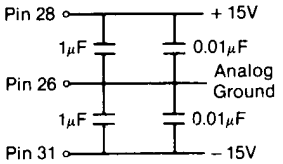
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies. Analog and digital grounds (pins 15 and 26) are not connected to each other internally and must be tied together as close to the package as possible, preferably through a large analog ground plane underneath the package. If these commons must be run separately, a nonpolarized, 0.01 to 0.1μF bypass capacitor should be connected between pins 15 and 26 as close to the package as possible and wide conductor runs should be used.

Coupling between the analog inputs and digital signals should be minimized to reduce noise pickup. The Summing Junction (pin 22) is the direct input to the internal comparator and is particularly noise susceptible. In bipolar operation, where pin 22 is connected to pin 23, a short jumper should be used, and when external offset adjustment is employed, the 1.8 megohm resistor should be located as close to the package as possible.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the device package. For optimum results, 1μF capacitors paralleled by 0.01μF ceramic capacitors should be connected as shown in the diagrams below. An additional 0.01μF ceramic bypass capacitor should be located close to the package connecting the gain adjust point (pin 27) to analog ground.





For normal 12-bit operation using the internal clock, Clock Adjust (pin 17) must be connected to Digital Ground (pin 15) and Short Cycle (pin 14) should be connected to +5V (pin 16).

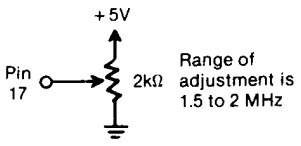
START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

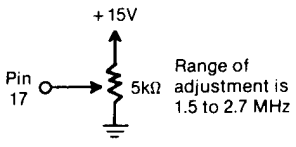
STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit of any conversion will not be valid until a maximum of 120nsec after the Status output has gone low.

SHORT CYCLING—For applications requiring less than 12 bits resolution, these converters can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. The connections shown below both increase the clock rate and truncate the converter to provide the minimum conversion time for a given resolution.

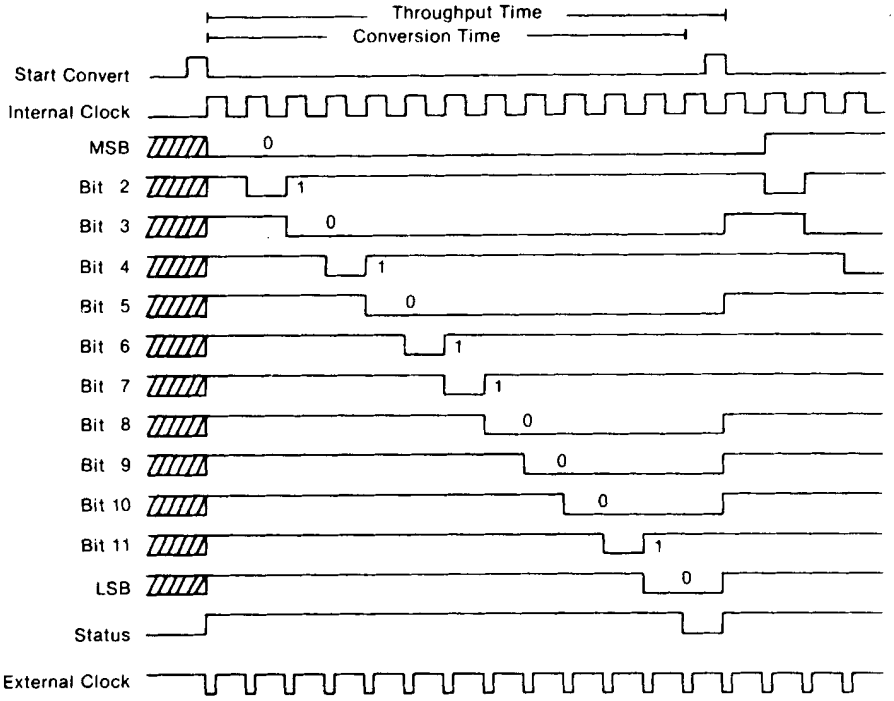
Resolution (Bits)	12	10	8
Connect Pin 17 to Pin	15	16	28
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μsec)	8	5	3
Clock Speed (MHz)	1.5	2	2.7

CLOCK RATE—The internal clock is preset to approximately 1.5 MHz and can be adjusted over a range of 1.5 to 2.7 MHz. To adjust the internal clock, a multiturn pot (TCR of 100ppm/°C or less) is connected to pin 17 as shown in the diagrams below.





TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Conversion time is defined as the width of the Status pulse.
2. The Start Convert command must be at least 50nsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. The delay from the falling edge of the Start Convert signal to Status actually rising to a "1" may be 100nsec.
5. Parallel data will be valid 120nsec after the Status (E.O.C.) output goes low and will remain valid until another conversion is initiated.
6. The delay from clock to serial data valid will be a maximum of 140nsec from a rising internal clock edge or a maximum of 200nsec from a falling external clock edge.
7. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See External Clock section.
8. Once a conversion has begun, a second start pulse will not reset the converter. See Start Convert section.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

EXTERNAL CLOCK—An external clock may be connected to the Start Convert input. This external clock must consist of negative going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. In this mode of operation, the converter will provide a continuous string of conversions each of which begins on the first falling edge of the external clock after Status (E.O.C.) has gone low.

INTERNAL BUFFER AMPLIFIER—ADC87 provides a user-optional internal buffer amplifier. Use of this buffer amplifier provides an input impedance greater than 100MΩ allowing the A/D to be driven from high impedance sources or directly from an analog multiplexer. When using the optional buffer amplifier, a 2μsec delay must be provided to allow the amplifier to settle prior to triggering the Start Convert input. If the buffer amplifier is not required, its input should be connected to analog ground to avoid introducing noise into the converter.

USING A TRACK/HOLD AMPLIFIER WITH AN ADC87—When using a track-hold (T/H) amplifier with an ADC87, the T/H can be driven directly (or inverted) from the A/D's Start Convert signal. When the Start is high prior to the beginning of a conversion, the T/H can be in the tracking or signal acquisition mode. The falling edge of the start signal initiates the conversion and simultaneously commands the T/H into the hold mode. The MSB output will be set to its final value one internal clock period later (approximately 0.67μsec), and the sample-to-hold transient of the chosen T/H should have settled to within ±0.01%FSR of its final value by that time. The width of the start convert pulse may have to be lengthened to accommodate the acquisition time spec of the chosen T/H.

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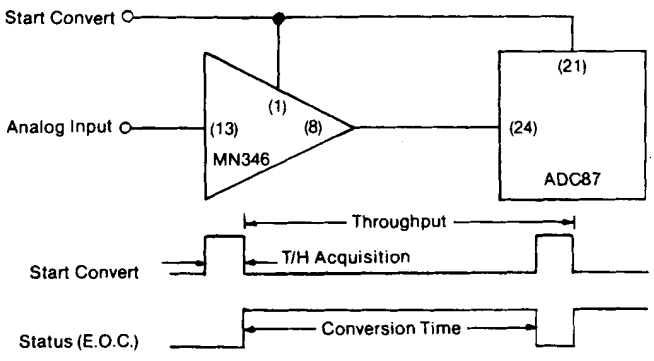
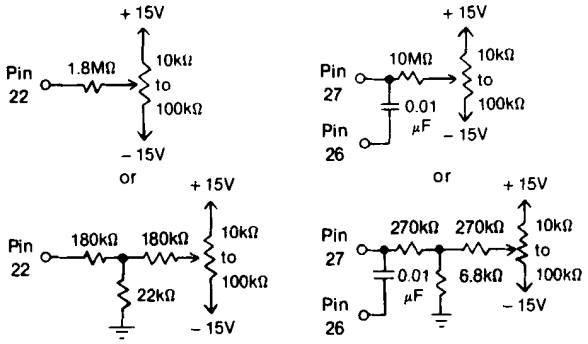


Throughput Rate	100kHz
T/H Acquisition Time	2μsec
A/D Conversion Time	8μsec

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS—Initial offset and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warm-up, and to avoid interaction, offset should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 22 should be connected as described in the Input Range Selection section and a 0.01μF capacitor should be connected from pin 27 to pin 26.

OFFSET ADJUSTMENTS—Connect the offset potentiometer as shown and apply the input voltage at which the 1111 1111 1110 to 1111 1111 1111 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the offset potentiometer until all the output bits are "1" and the LSB "flickers" on and off.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply the input voltage at which the 0000 0000 0001 to 0000 0000 0000 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the gain potentiometer until all the output bits are "0" and the LSB "flickers" on and off. A 0.01μF capacitor should be connected from Gain Adjust (pin 27) to Analog Ground (pin 26).



INPUT RANGE SELECTION

Pin Connections	Analog Input Voltage Range				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
FOR NORMAL INPUT					
Input Impedance (kΩ)	2.5	5	2.5	5	10
Connect Pin 23 to Pin	26	26	22	22	22
Connect Pin 25 to Pin	22	Open	22	Open	Input Signal
Connect Pin 30 to Pin	26	26	26	26	26
Connect Input to Pin	24	24	24	24	25
FOR BUFFERED INPUT					
Input Impedance (MΩ)	100	100	100	100	100
Connect Pin 23 to Pin	26	26	22	22	22
Connect Pin 25 to Pin	22	Open	22	Open	29
Connect Pin 29 to Pin	24	24	24	24	25
Connect Input to Pin	30	30	30	30	30

DIGITAL OUTPUT CODING

Analog Input Voltage Range					Digital Outputs
0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB LSB
+5.0000	+10.0000	+2.5000	+5.0000	+10.0000	0000 0000 0000
+4.9982	+9.9963	+2.4982	+4.9963	+9.9927	0000 0000 000Ø*
+2.5006	+5.0012	+0.0006	+0.0012	+0.0024	0111 1111 111Ø*
+2.4994	+4.9988	−0.0006	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ*
+2.4982	+4.9963	−0.0018	−0.0037	−0.0073	1000 0000 000Ø*
+0.0006	+0.0012	−2.4994	−4.9988	−9.9976	1111 1111 111Ø*
0.0000	0.0000	−2.5000	−5.0000	−10.0000	1111 1111 1111

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is complementary straight binary (CSB).
2. For bipolar input ranges, output coding is complementary offset binary (COB).
3. For bipolar input ranges, complementary two's complement coding (CTC) can be obtained by using the complement of the most significant bit MSB. $\overline{MSB}$ is available on pin 13. See Pin Designations.
4. For 0 to +5V or ±2.5V input ranges, 1LSB for 12 bits = 1.22mV. 1LSB for 10 bits = 4.88mV.
5. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 10 bits = 9.77mV.
6. For ±10V input range, 1LSB for 12 bits = 4.88mV. 1LSB for 10 bits = 19.5mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADC87 operating on its ±10V input range, the transition from digital output 1111 1111 1111 to 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of −9.9976 volts (−Full Scale +½LSB). Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "1's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input voltage of −0.0024 volts (−½LSB) and the 0000 0000 0001 to 0000 0000 0000 transition should occur at +9.9927 volts (+Full Scale −3/2LSB). An input more positive than +9.9927 volts will give all "0's".