

# MC74HCT74A

## Dual D Flip-Flop with Set and Reset with LSTTL Compatible Inputs

### High-Performance Silicon-Gate CMOS

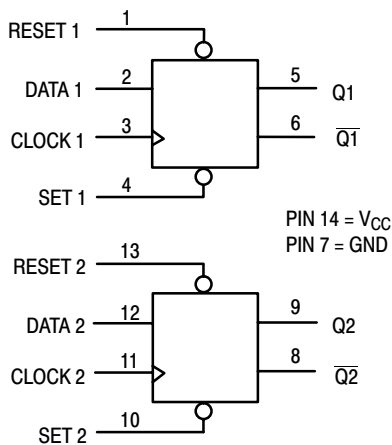
The MC74HCT74A is identical in pinout to the LS74. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and  $\bar{Q}$  outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- TTL NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 136 FETs or 34 Equivalent Gates
- Pb-Free Packages are Available\*

#### LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count†	34	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	.0075	pJ

†Equivalent to a two-input NAND gate.

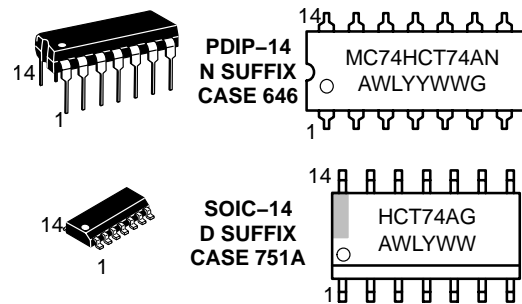
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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#### MARKING DIAGRAMS



A = Assembly Location  
 L, WL = Wafer Lot  
 Y, YY = Year  
 W, WW = Work Week  
 G = Pb-Free Package

#### PIN ASSIGNMENT

RESET 1	1	14	V <sub>CC</sub>
DATA 1	2	13	RESET 2
CLOCK 1	3	12	DATA 2
SET 1	4	11	CLOCK 2
Q1	5	10	SET 2
Q1-bar	6	9	Q2
GND	7	8	Q2-bar

#### FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↔	X	No Change	

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — Plastic DIP: -10mW/°C from 65° to 125°C

SOIC Package: -7mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	- 55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				- 55 to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
			4.5	3.98	3.84	3.7	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
			4.5	0.26	0.33	0.4	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	5.5	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	5.5	2.0	20	80	$\mu\text{A}$
$\Delta I_{CC}$	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or } GND, \text{ Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	$\geq -55^\circ\text{C}$	$25^\circ\text{C to } 125^\circ\text{C}$		mA
				2.9	2.4		

1. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		- 55 to 25°C	≤ 85°C	≤ 125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	24	30	36	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Set or Reset to Q or $\bar{Q}$ (Figures 2 and 4)	24	30	36	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF

2. For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

$C_{PD}$	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$		pF
		32		

3. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## TIMING REQUIREMENTS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Fig.	Guaranteed Limit						Units
			- 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
$t_{su}$	Minimum Setup Time, Data to Clock	3	15		19		22		ns
$t_h$	Minimum Hold Time, Clock to Data	3	3		3		3		ns
$t_{rec}$	Minimum Recovery Time, Set or Reset Inactive to Clock	2	6		8		9		ns
$t_w$	Minimum Pulse Width, Clock	1	15		19		22		ns
$t_w$	Minimum Pulse Width, Set or Reset	2	15		19		22		ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Times	1		500		500		500	ns

## ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT74AN	PDIP-14	500 Units / Rail
MC74HCT74ANG	PDIP-14 (Pb-Free)	500 Units / Rail
MC74HCT74AD	SOIC-14	55 Units / Rail
MC74HCT74ADG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74HCT74ADR2	SOIC-14	2500 Units / Reel
MC74HCT74ADR2G	SOIC-14 (Pb-Free)	2500 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## SWITCHING WAVEFORMS

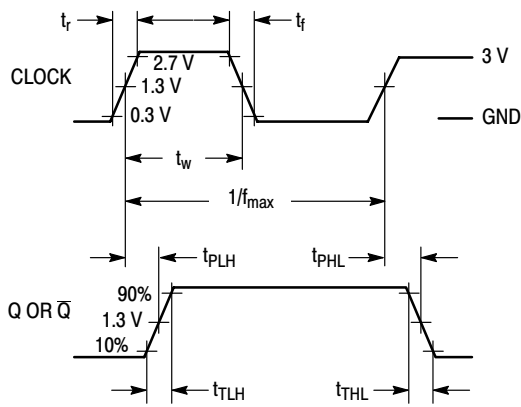


Figure 1.

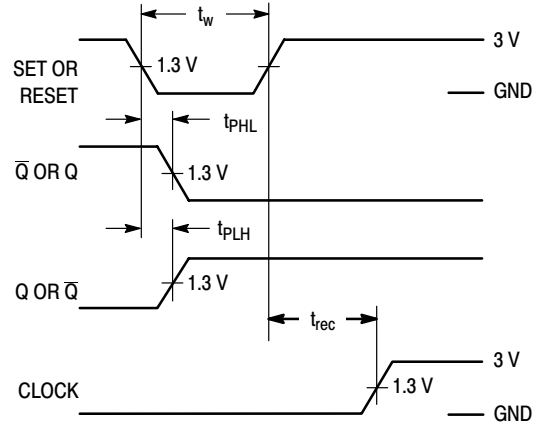


Figure 2.

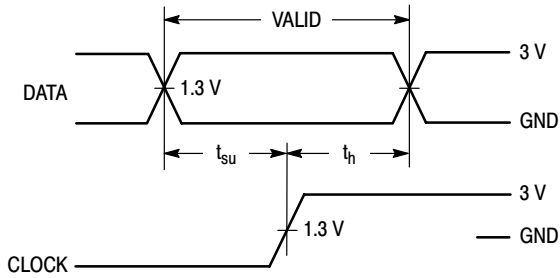
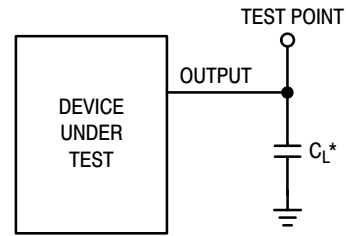


Figure 3.



\*Includes all probe and jig capacitance

Figure 5.

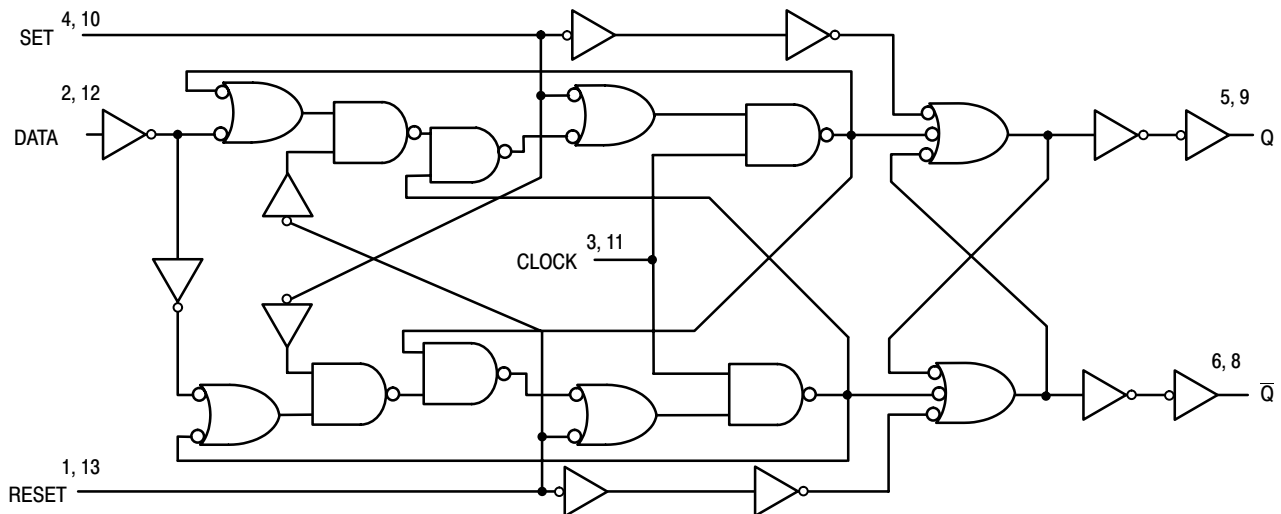
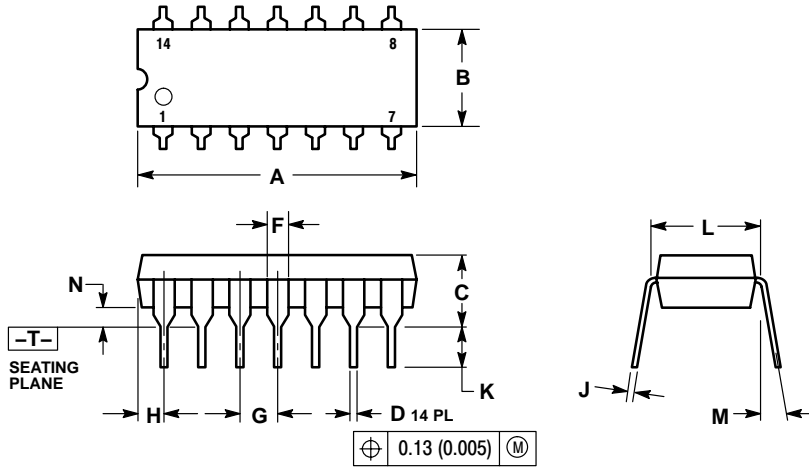


Figure 4. Expanded Logic Diagram

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## PACKAGE DIMENSIONS

PDIP-14  
N SUFFIX  
CASE 646-06  
ISSUE N



NOTES:

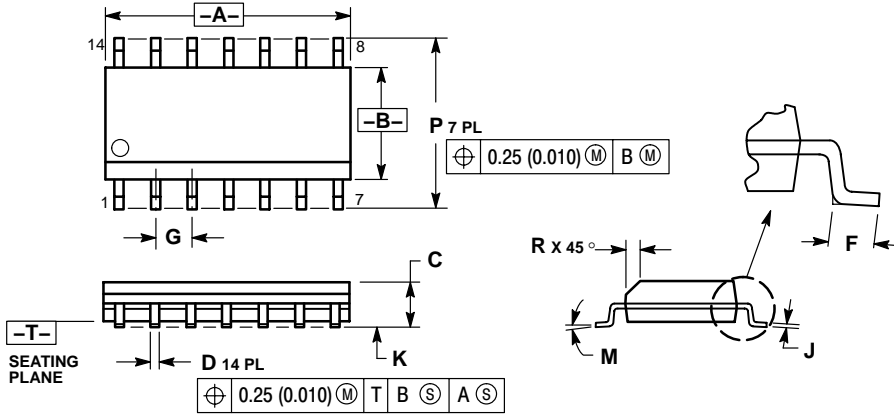
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

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## PACKAGE DIMENSIONS

SOIC-14  
D SUFFIX  
CASE 751A-03  
ISSUE G



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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